A Broadband Monolithic S-band Class-E Power Amplifier

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Abstract: This paper describes what is believed to be the first successful design and fabrication of a highly efficient broadband monolithic class-E power amplifier that operates at S-band and employs a 0.3 um x 1000 um pHEMT device. The amplifier measured performance shows a peak Power Added Efficiency (PAE) of 90% and a peak output power of greater than 23 dBm at 3.25 GHz.

I. Introduction

Highly efficient microwave and RF power amplifiers are required for many commercial as well as defense system applications. These include wireless LANs, cellular phones and telecommunication systems as well as advanced air-borne active phased array radar systems.

The design of class-E amplifiers is based on using a series or parallel resonant load network. The current and voltage time-waveforms at the active device output terminal are optimized in such a way to minimize the DC power dissipation within it. The active device acts as a switch, driven by the RF input signal to ON and OFF conditions. The ideal AC load lines for switching transistors (class D, E, F) are shown in Figure 1(b). It can be seen that the operating point moves along the Vds and Idss axes; i.e. the device is either OFF (in the saturated region) or ON (in the linear region). Under this ideal switching operation, the output voltage and current waveforms at the device output terminal do not simultaneously exist and therefore, the dissipated energy within the device is zero leading to 100% theoretical power conversion efficiency.

With the advent of active device performance, non-linear modeling and monolithic circuit technology in the last few years, significant progress has been noted towards the development of high efficiency RF and microwave components. In the case of class-E high efficiency power amplifiers, the circuit designers have pushed the useful operating frequency of these circuits to ever-higher frequencies [1-3].

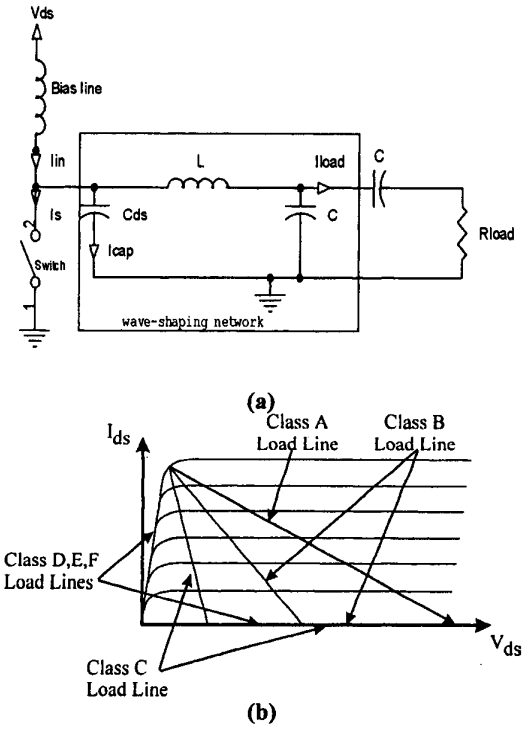

Figure 1: (a) Ideal switching amplifier circuit (shunt load). (b) Ideal transistor load lines for several classes of operation.

In this work, we have made a special effort in optimizing the amplifier's lumped-element load network in a CPW environment for the highest PAE attainable while maintaining a minimum of 23 dBm output power. All aspects of non-linear device modeling and circuit simulations, including time domain analysis, Harmonic Balance (HB) analysis and large signal stability analysis, were performed using Agilent ICCAP and ADS simulators respectively [4].

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II. Design Methodology

The detailed analysis and derivation of the ideal load networks for class-E amplifiers are fully discussed elsewhere [1]. Knowing the device drain to source capacitance (C_{ds}) and the drain voltage (V_{ds}), an approximate maximum frequency (f_{max}) for class-E operation can be obtained. Similarly, assuming a load resistance of 50 ohms, approximate values for the circuit elements (L and C) of the shunt load network shown in Figure 1(a) can be obtained by using the following expressions:

$$f_{max} = \frac{I_{max}}{56.5 C_{ds}},$$

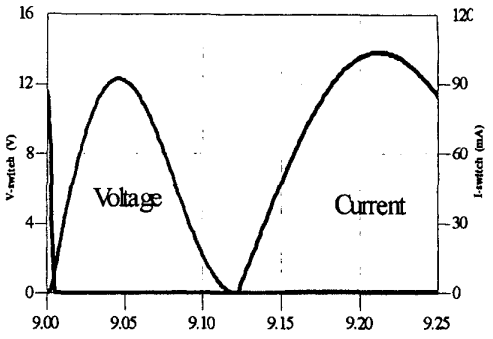
$$L = \frac{0.28}{\omega^2 C_{ds}}\left[\sin\theta_0 + \cos\theta_0 \sqrt{\frac{\omega_s C_{ds} R}{k_0 \cos\theta} - 1}\right]$$

$$C = \frac{1}{\omega_s R}\sqrt{\frac{\omega_s C_{ds} R}{k_0 \cos\theta_0 - 1}}$$

Where: $k_0 = 0.28$, $\theta_0 = 49.05°$, $\omega = 2\pi f_{max}$

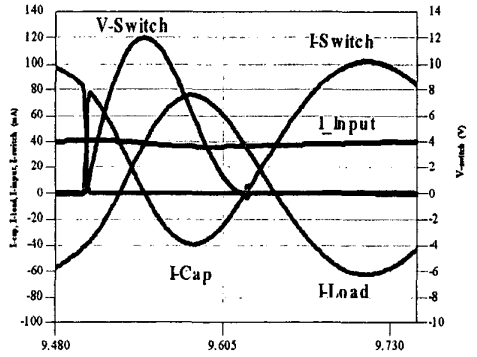
Having obtained the starting values for the load network, a time domain simulation was performed to optimize the current and voltage waveforms at appropriate terminals of the ideal class-E circuit shown in Figure 1(a).

Figure 2 shows the simulation results for the circuit after optimization of the load network. The voltage waveform across the switch rises slowly at switch-off and falls to zero at the end of the half-cycle. It also has a zero rate of change at the end of half-cycle, thereby ensuring a "soft" turn-on condition. The voltage across the switch when it is off is defined by the integral of the current flowing through C_{ds}. The phase shift introduced by the LC circuit adjusts the point at which the current is diverted from the switch to the capacitor C_{ds}. Therefore, to ensure class-E operation, it is essential that the integral of capacitor current over the half-cycle is zero and that the capacitance current has dropped to zero by the end of the half-cycle. Figure 3 shows that the optimized current and voltage waveforms comply with the aforementioned criteria for the class-E amplifiers.



Time (nSec)

Figure 2: Switch voltage and current waveforms for circuit (1a)



Time (nSec)

Figure 3: Current-voltage waveforms for circuit (1a)

The majority of the existing non-linear pHEMT models available in the commercial circuit simulators are not suitable for modeling class-E circuits. For accurate modeling of switching mode amplifiers, the model should have the following important properties:

- Bias dependency of drain-to-source $C_{ds}(V_{ds},V_{gs})$ and gate-to-drain C_{gd} (V_{ds},V_{gs}) capacitances
- Bias dependency of input channel resistance R_i (V_{ds},V_{gs})
- Bias dependency of output channel resistance $R_{ds}(V_{ds},V_{gs})$
- A two current generator dispersion model for accurate simulation of R_{ds}

Any non-linear models that model the dispersive behavior of the output resistance by a simple series

resistor-capacitor network, connected in parallel to the standard output network, should be used with care. In such a case, the loading effect of the series resistor-capacitor network on the output resistance should be removed.

After careful observation of the available non-linear models, we decided on the EEHEMT model [1] as a suitable choice for the non-linear simulation of class-E amplifiers. The most distinguishing features of this model for class-E are the ability to model R_{ds}(Vds, Vgs) and its dispersion effect, as well as the bias dependencies of the device capacitances.

Our design objective was to develop a highly efficient class-E monolithic amplifier operating over 3-5 GHz using a 0.3 um x 1000 um pHEMT device. The design process starts by generating the large signal S-parameters of the device over the desired RF input drive and frequency band while the device stability is assured by conventional circuit techniques. The next stage is to design the input-matching network for the amplifier by providing a conjugate match to the large signal S11 over the frequency band of interest. Figure 4 shows the final schematic circuit of the CPW monolithic amplifier.

Figure 5 depicts the simulated voltage and current waveforms at the pHEMT output terminals. The waveforms confirm the switching mode behavior of the pHEMT, a condition that is necessary for class-E operation of the amplifier.

III. Measured Performance

The completed monolithic amplifier chip is shown in Figure 6. A primitive layout was used in this first iteration to assure the accuracy of the complex load.

Figure 7 depicts the measured amplifier power added efficiency (PAE) for different RF input drive levels. PAE of greater than 70% over 3.0-3.7 GHz is obtained for 15.0 dbm input power drive, and a peak PAE of more than 90% is obtained at around 3.25 GHz when the amplifier is driven by only 12.0 dbm of input power.

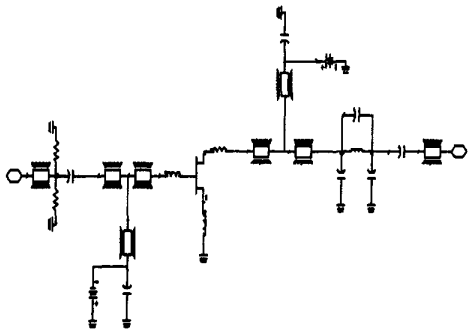


Figure 4: S-band Class-E amplifier circuit

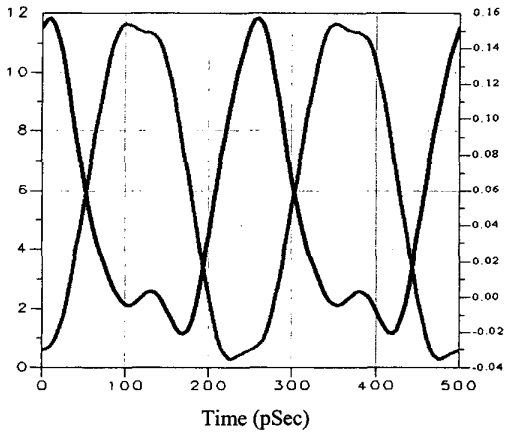


Figure 5: Simulated waveforms of the class-E amplifier

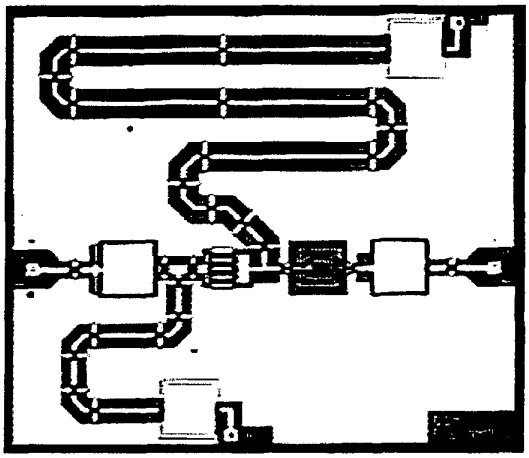


Figure 6: MMIC Amplifier chip

Figure 8 shows the measured amplifier output power for different values of RF input drive levels (-1-12 dBm) over 2-6 GHz. As it can be seen, a broadband output power is obtained indicating the broadband capability of class-E operation. At 3.25 GHz, the output power is more than 23.0 dbm for an input drive level of 12.0 dbm.

Figure 9 shows the measured output power, PAE, and gain vs. input power at 3.25 GHz. A maximum PAE of 92%, and an output power of greater than 23 dBm is obtained at P_{in}=12 dBm.

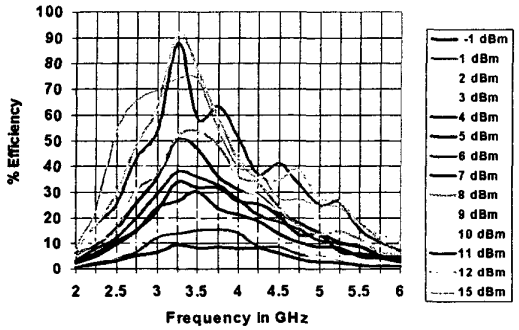


Figure 7: Measured PAE vs. frequency
Bias (Vds=5V, Vgs=-1V)

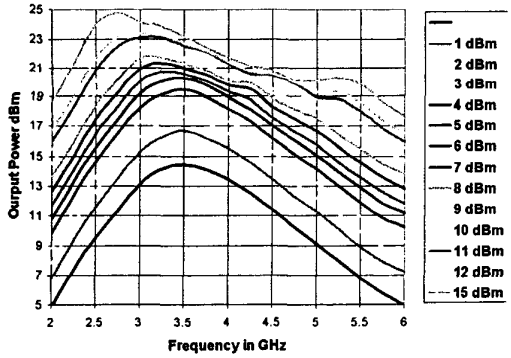


Figure 8: Measured output power, vs. frequency
Bias (Vds=5V, Vgs=-1V)

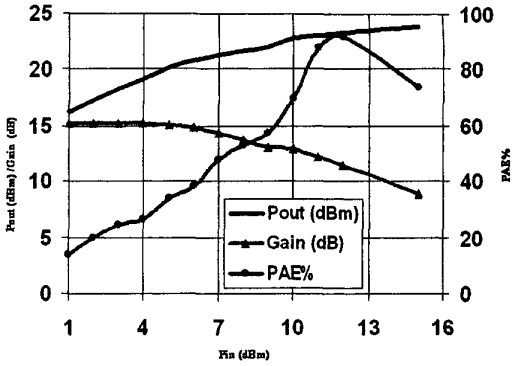


Figure 9: Measured output power, PAE, and gain vs. input power at 3.25 GHz.

IV. Conclusions

The first successful design and fabrication of a highly efficient S-band monolithic CPW class-E amplifier that employs a 0.3 um x 1000 um pHEMT device has been reported. The amplifier measured performance shows a peak Power Added Efficiency (PAE) of more than 90% and a peak output power of greater than 23 dBm at 3.25 GHz

References

[1] T.B. Mader and Z.B. Popovic, "The Transmission-Line High-Efficiency Class-E Amplifier", 1999 IEEE M&GWL, Vol.5, N0.9, pp.290-292, Sept. 1995.

[2] R. Tayrani., "A Monolithic X-band Class-E Amplifier", IEEE GaAs IC Symposium Digest 2001, pp.205-208

[3] T. Quach, et al., "Broadband Class-E Power Amplifier for Space Radar Application", IEEE GaAs IC Symposium Digest 2001, pp.209-212

[4] Agilent Advanced Design Systems (ADS), V.1.7, & Agilent ICCAP, V.5.4.